PATENT
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REACTIVE PRECLEAN PRIOR TO METALLIZATION FOR SUB-QUARTER MICRON APPLICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of co-pending U.S. patent application, Serial No. 09/617,522, filed on July 14, 2000, now Patent 6,693,030 which is a continuation of U.S. Patent No. 6,107,192 filed on December 30, 1997. Each of the aforementioned related patent applications is herein incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a metallization method for manufacturing semiconductor devices. More particularly, the present invention relates to precleaning of submicron features prior to metallization.

Description of the Related Art

[0003] Sub-half micron multilevel metallization is one of the key technologies for the next generation of very large scale integration (VLSI). The multilevel interconnects that lie at the heart of this technology require planarization of interconnect features formed in high aspect ratio apertures, including contacts, vias, lines or other features. Reliable formation of these interconnect features is very important to the success of VLSI and to the continued effort to increase circuit density and quality on individual substrates and die.

[0004] The increase in circuit densities primarily results from a decrease in the widths of vias, contacts and other features as well as a decrease in the thickness of dielectric materials between these features. Cleaning of the features to remove contaminants prior to metallization is required to improve device integrity. The decrease in width of the features results in larger aspect ratios for the features and increas d difficulty in cleaning the features prior to filling the features with m tal or